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R. G. Nelson
J. H. Nuckols

A Hardware Implementation of the ATCRBS Reply Processor Used in DABS

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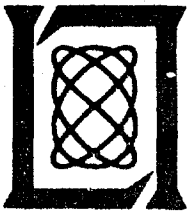

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16. Abstract

A special-purpose digital hardware processor, which implements the ATCRBS Reply Processing algorithms designed for use in the Discrete Address Beacon System (DABS) has been developed and used in two DABS-related programs. This report gives a detailed functional description of this processor as implemented by Lincoln Laboratory. With minor modifications it could serve as the ATCRBS Reply Processor for a Beacon Collision Avoidance System.

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1. INTRODUCTION

The ATCRBS reply processor described in this report was originally designed for use in the Discrete Address Beacon System (DABS). It has been previously described in functional terms in the DABS Engineering Requirement [Ref. 1], and its principal of operation and role in the overall ATCRBS processing function has been the topic of a previous ATC report [Ref. 2]. This reply processor has been implemented both in the Lincoln Laboratory DABS Experimental Facility (DABSEF) and the ATCRBS Monopulse Processing System (AMPS) with excellent results [Ref. 3]. With some minor modifications, it could also serve as the basis for a design of an ATCRBS reply processor for an airborne Beacon Collision Avoidance System (BCAS) employing ATCRBS signal formats.

The organization and breakdown of the processor subsystems described in this report reflect the physical partitioning of the hardware reply processors built at Lincoln Laboratory. Other arrangements of the hardware subsystems could be used and many of the hardware functions could be replaced by equivalent software operations if warranted by the constraints of the application.

2. OVERVIEW OF THE REPLY PROCESSING FUNCTION

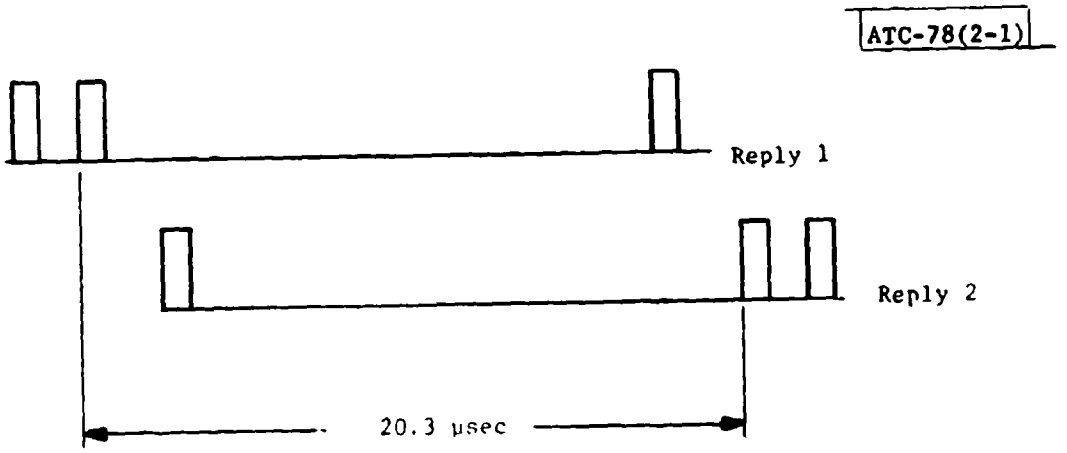
The function of the reply processor is to identify all ATCRBS replies by searching the received pulse train for framing pulse pairs and then to decide which (if any) of the code pulses are present for each reply. The hardware also determines the range of each reply, from the time of arrival of the F1 pulse, and the azimuth of each reply, from the monopulse samples of all pulses received.

2.1 Reply Detection

A candidate ATCRBS reply is declared whenever two pulses separated by approximately 20.3 microseconds ("framing" pulses) are located in the input pulse stream. The candidate reply is accepted as a valid reply provided it meets both of the following criteria:

a. At least one of the framing pulses is received in the antenna mainbeam and is not garbled. This condition is implemented by receive sidelobe suppression (RSLS) circuitry that identifies each pulse received in a sidelobe of the antenna.

b. The reply is not a phantom. A phantom reply is defined to be one created by pulses from two valid replies. An example is illustrated in Fig. 2-1. When two replies overlap properly, a pulse of the first reply can be separated from one of the second by the 20.3 microsecond interval that characterizes framing pulses, thereby creating an intermediate candidate reply. The reply processor eliminates the middle reply whenever three candidate mainbeam replies are found whose relative times satisfy the phantom conditions.



Pulse from Reply 1 and pulse from Reply 2 form a phantom bracket pair.

Fig. 2-1. Creation of a phantom reply.

2.2 Reply Decoding and Confidence Bits

Once a reply has been detected, the reply processing hardware must determine, for each of the twelve code positions, whether or not a pulse exists in that position, and if so, whether or not it belongs to that reply.

Rather than force a possibly wrong guess to be made, for each code bit decision, a corresponding confidence decision, high or low, is made. When the decision is straightforward, the confidence flag is set ('1'); when the decision is ambiguous, the best estimate is made, but the confidence flag is turned off ('0').

The rules for determing what values of code and confidence to assign to a given pulse position of a given reply are the following:

HO: A high confidence 0 is declared whenever no pulse is detected in the code position.

H1: A high confidence 1 is declared whenever a mainbeam pulse is detected in the code position that correlates in azimuth with the reply reference azimuth and fails to correlate with the reference of every other garbling reply (if any).

LO: A low confidence 0 is declared whenever either (a) a sidelobe pulse is detected in the code position, or (b) a mainbeam pulse is detected that fails to correlate in azimuth with the reply reference but succeeds in correlating with the reply reference of a garbling reply.

L1: A low confidence 1 is declared whenever a mainbeam pulse exists in the code position that either (a) fails to correlate in azimuth with the reply reference and with the references of all other garbling replies (if any), or (b) correlates successfully with both the reply reference and the reference of one or more garbling replies.

An example of the application of these rules in a garbling situation is presented in Fig. 2-2.

The reference azimuth for a reply is initially set to the azimuth of the F1 framing pulse of the reply. However, if this pulse is located in a garble region the azimuth of the F2 pulse is used. It should be noted that these reference azimuth selection rules permit a sidelobe pulse to be chosen. The reply correlation software implementation discards any reply each of whose framing pulses is either garbled or sidelobe. The reply reference azimuth is updated each time a high confidence 1 is declared for the reply (code pulse or framing pulse) through simple averaging of the old reference with the new sample.

2.3 Reply Processor Outputs

For each interrogation sweep, the reply processor transmits to the ATCRBS software the following two items of information:

a. Mode of the sweep (A, C, or 2).

b. Antenna boresight azimuth.

In addition, for each reply declared by the reply processor, the following set of information is provided:

a. Reply range.

b. Reply boresight azimuth.

c. Reply monopulse reference.

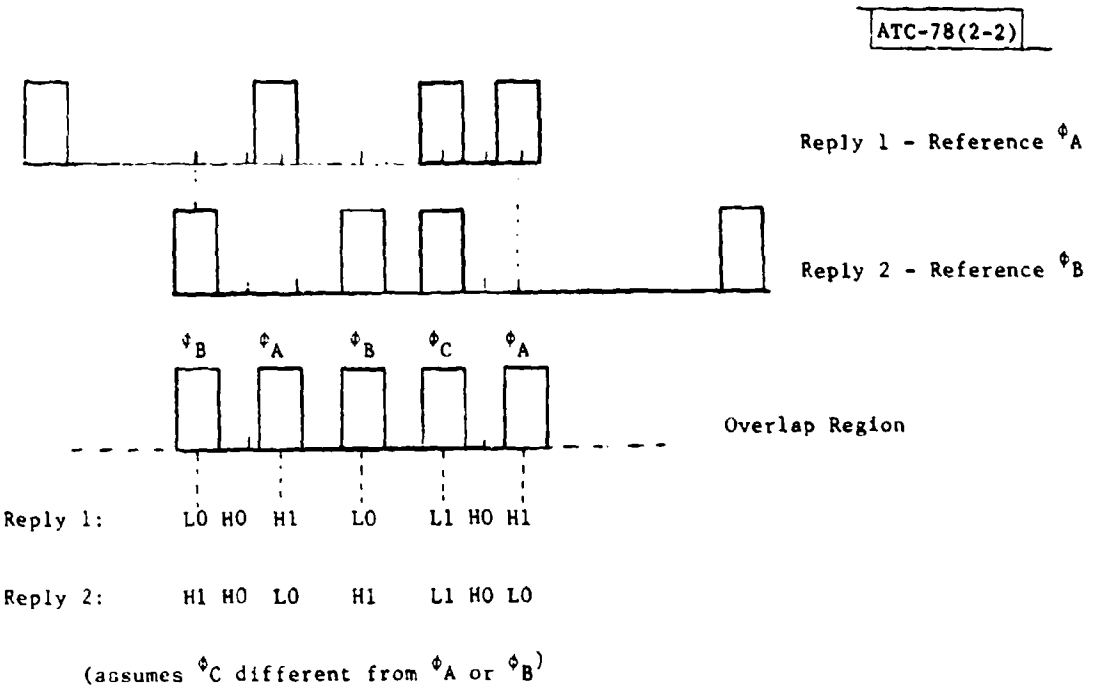


Fig. 2-2. Confidence bit decisions.

d. Reply code.

e. Reply code confidence.

f. Special implementation dependent reply attributes.

The range is given in time counts from sweep interrogation until reception of the F1 pulse. The reply boresight azimuth is the antenna azimuth at the time the reply was received.

3. BLOCK DIAGRAM AND SIGNAL FLOW

The ATCRBS Reply Processor consists of a number of functional subsystems. These subsystems and the functional relationship between them are shown in Fig. 3-1. In this figure, each subsystem is represented by a solid-lined block.

Four two-level quantized video signals are applied to the ATCRBS reply processor at the video digitizer.

a. A quantized sum video signal which indicates when the received log Σ video signal exceeds a preset minimum triggering level (MTL), denoted as QΣA.

b. Quantized positive and quantized negative slope signals which indicate when the log Σ signal exceeds a preset rate of change in the positive and negative directions, respectively, denoted as QΣPS and QΣNS.

c. A quantized video signal associated with each log Σ pulse which indicates whether the corresponding log Σ pulse was received in the antenna mainbeam or a sidelobe, denoted as QRSLS.

These four signals normally are used to produce actual leading edge (ALE), actual trailing edge (ATE), and sampled quantized sum video (SQΣA) pulses for each log Σ pulse that is received. The width of the SQΣA pulse is determined precisely by the relative position of the ALE and ATE pulses.

The outputs of the video digitizer are used by the pseudo leading edge (LE) pulse generator to measure the pulse width of each log Σ pulse. Measured

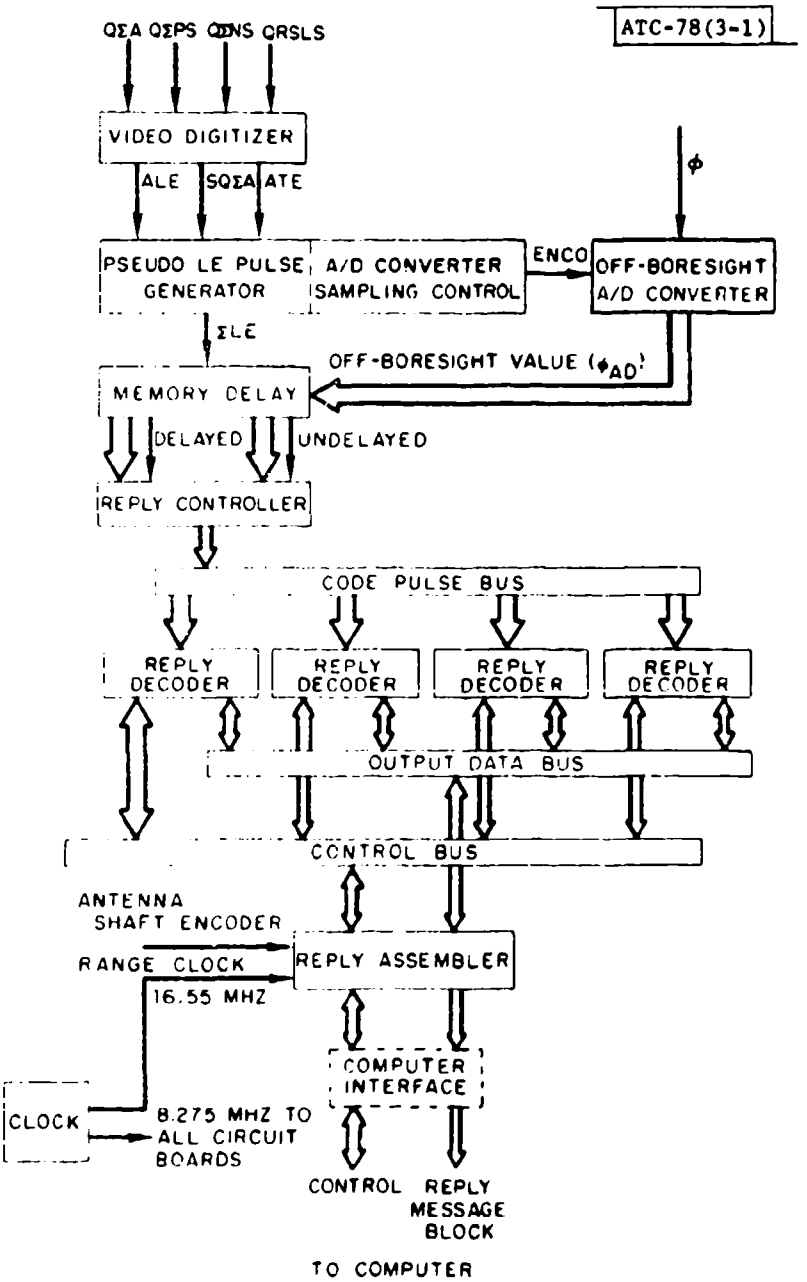


Fig. 3-1. ATCRBS reply processor, block diagram.

pulse-width values which exceed the standard ATCRBS value indicate that one or more leading edges were not detected. Consequently, the missing leading edge pulses (pseudo LE pulses) are inserted into the leading edge pulse stream, wherever appropriate, by the pseudo LE pulse generator.

In addition to inserting pseudo LE pulses, the A/D converter sampling control portion of this circuit provides the necessary encode commands (ENCO) to the A/D converter. The converter measures the magnitude of the monopulse off-boresight reply-code signal (ϕ) associated with each log Σ pulse and delivers this value (ϕ_{AD}) to the memory delay circuit.

The sum leading edge pulse output (ΣLE) from the pseudo LE pulse generator, and the associated monopulse reply-code pulse value (ϕ_{AD}) from the A/D converter enter the memory delay circuit and are divided into two lines. One line goes directly to the reply controller while the other line goes through a 20.3 microsecond delay before entering the reply controller.

At the reply controller, the leading edge signals on the delayed and undelayed lines are compared for the simultaneous presence of a pulse on each line, i.e., an F_1 pulse on the delayed line and an F_2 pulse on the undelayed line. This condition signifies the detection of an ATCRBS reply bracket pair, and the reply controller assigns the corresponding reply pulses appearing on the code pulse bus to one of the idle reply decoders by activating that reply decoder.

Before the reply is assigned, the reply controller selects either the F_1 or F_2 pulse as the monopulse reference value against which the subsequent pulses are correlated for decoding and monopulse estimation. The F_1 pulse is

selected unless this pulse is garbled by a previous reply. After a reply decoder begins to process a reply, the reply controller assists the reply decoder by performing military ident/emergency decoding and phantom bracket detection when appropriate.

Actual decoding of individual replies is performed by the reply decoders. Up to four overlapping replies may be decoded. A confidence bit is associated with each decoded bit to indicate the level of certainty which the decoding algorithm has in its own code-bit decision. The decoders also perform the task of reply azimuth estimation by forming a weighted average of the individual code-pulse azimuth estimates which correlate with the monopulse reference pulse. After the pulse decoding and azimuth estimating are completed, the reply decoder notifies the reply assembler that the reply data are ready.

After the reply assembler receives a reply-ready notification, it coordinates the collection and formatting of data from the reply decoder, the range counter, and the antenna azimuth register. When the collecting and formatting are completed, the reply assembler transfers a completed message block to the computer via a computer interface. The interface provides the channeling and intercommunication between the computer and the reply assembler which is necessary in implementing the transfer of the message data to the computer. The computer interface is not described in this report because its design is implementation dependent.

Digital synchronization within the ATCRBS reply processor is provided by the clock which delivers 8.276-MHz timing pulses to every circuit function within the processor, plus 16.552-MHz timing pulses to the reply assembler for range counting.

4. VIDEO DIGITIZER

The primary function of the video digitizer is to convert the quantized positive slope, negative slope, and sum video inputs into quantized leading edge, quantized trailing edge and sampled quantized sum video pulse outputs for use by the pseudo leading edge detector. A functional block diagram of the video digitizer is presented in Fig. 4-1.

4.1 Circuit Initialization

At the beginning of the reply listening interval following the transmission of an interrogation, a range gate signal is received and used to enable specific reply processor functions. On the video digitizer the range gate signal enables the leading edge pulse generator, and also is used to generate a reset pulse and a System Reset Clear (SRC) pulse. At the beginning of each reply listening interval, the reset pulse clears the busy flip-flop in each of the four reply decoder while the SRC pulse clears the buffer controller in the memory.

4.2 Leading Edge Pulses

After a reply is received by the sensor, a stream of quantized positive slope (QΣPS), quantized negative slope (QΣNS), quantized sum video (QΣA), and quantized received sidelobe suppression (QRSLS) pulses are delivered to the video pulse quantizer. The transition of a positive slope to no slope condition and the presence of quantized sum video (QΣA) at the input of the

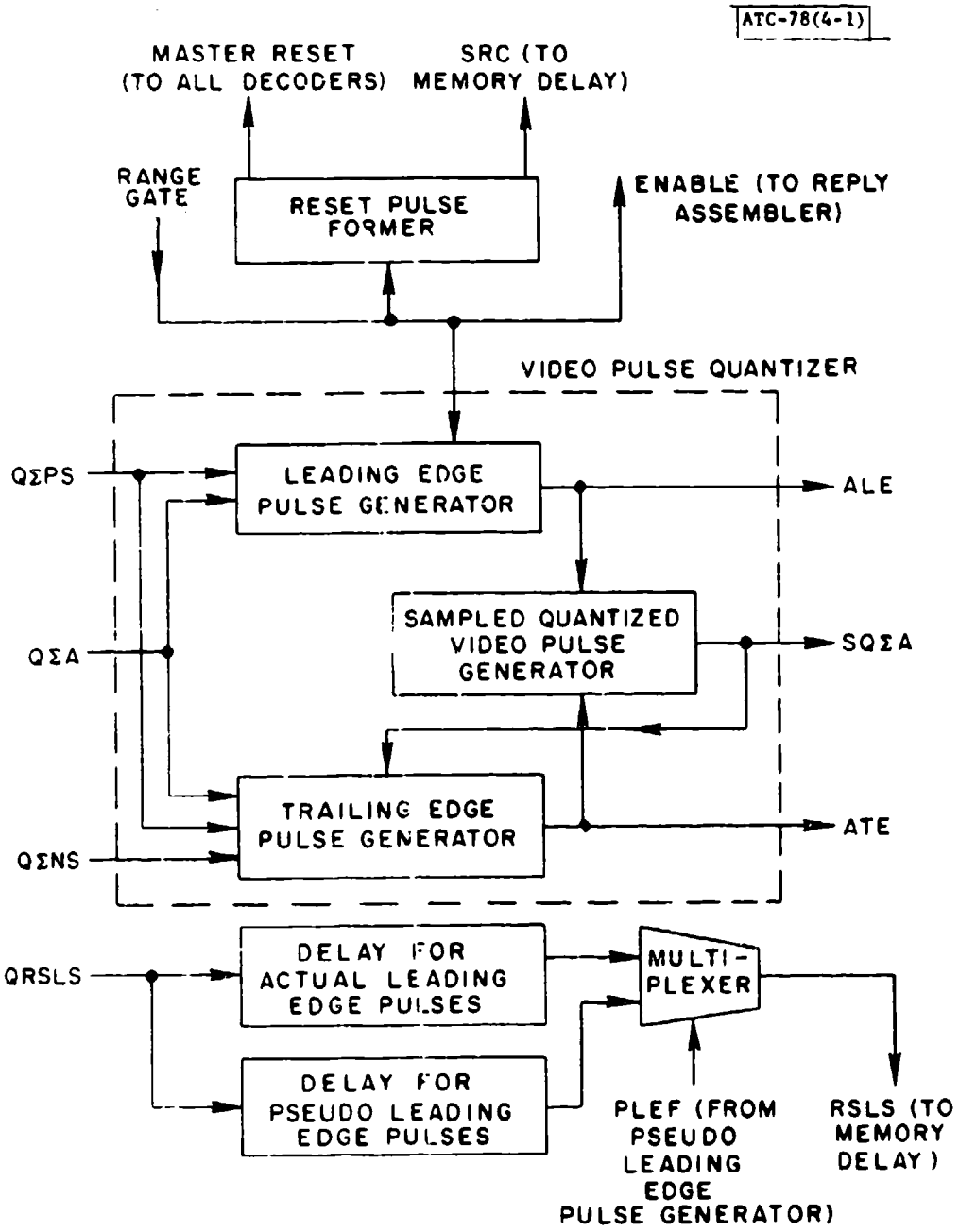


Fig. 4-1. Video digitizer, block diagram.

leading edge (LE) pulse generator produces an actual leading edge (ALE) pulse. The width of this ALE pulse is identical to that of a clock pulse. The ALE pulse then is delivered to the sampled quantized sum video pulse generator to initiate its operation, and to the pseudo LE pulse generator for additional processing.

4.3 Sampled Quantized Sum Video Pulses

When the sampled quantized sum video (SQΣV) generator is enabled by the LE pulse generator, the SQΣV pulse generator raises its output line to a high level. This high level is maintained until an actual trailing edge (ATE) pulse is received from the trailing edge (TE) pulse generator, at which time the output line is reduced to a low level. In this manner, the SQΣA pulse width is made equal to the duration between the ALE and ATE pulses. When the output line of the SQΣV pulse generator goes high, the TE pulse generator becomes enabled and remains in this condition for the duration of the SQΣA pulse. In addition, the SQΣV pulse generator output is forwarded to the pseudo LE generator where further processing of the SQΣA pulse is performed.

4.4 Trailing Edge Pulses

When the trailing edge (TE) pulse generator is enabled by the SQΣV pulse generator, it examines the quantized negative slope (QΣNS) pulse in conjunction with the QΣPS and QΣA pulses for the following conditions:

a. $Q\Sigma A(t_2) = 0$.

b. $Q\Sigma NS(t_2-1) = 0$, $Q\Sigma NS(t_2) = 1$, and $Q\Sigma A(t_2+1) = 0$.

c. $Q\Sigma NS(t_2-1) = 0$, $Q\Sigma NS(t_2) = 1$, $Q\Sigma NS(t_2+1) = 1$, and $Q\Sigma A(t_2+2) = 0$.

d. $Q\Sigma NS(t_2-1) = 0$, $Q\Sigma NS(t_2) = 1$, $Q\Sigma NS(t_2+1) = 1$, and $Q\Sigma NS(t_2+2) = 1$.

e. $Q\Sigma NS(t_2-1) = 0$, $Q\Sigma NS(t_2) = 1$, $Q\Sigma NS(t_2+1) = 1$, and $Q\Sigma PS(t_2+2) = 1$.

where t_2 is the trailing edge time, and the deviations from this time are in clock-pulse intervals.

When any one of these conditions are met, an actual trailing edge (ATE) pulse is generated. This pulse then is applied to the SQΣV pulse generator to produce the trailing edge of the SQΣA pulse. In addition, the ATE pulse is forwarded to the pseudo LE pulse generator for futher processing.

4.5 Receive Sidelobe Suppression

The quantized receive sidelobe suppression (QRSLS) signal line primarily is used to flag pulses that were received in an antenna sidelobe. Absence of a pulse on this line while a reply pulse is present indicates that the reply was received in the antenna sidelobe.

Every actual leading edge (ALE) and pseudo leading edge (PLE) pulse (PLE pulses are described in Section 5) must enter the memory delay precisely in coincidence with its associated RSLS flag. Because some delays are encountered in processing the ALE and PLE pulses before they are applied to the memory delay the QRSLS pulses are delayed appropriately before being

applied as flags (RSLSF) to the memory delay. Two delay lines are provided for this purpose: one is associated with an ALE pulse, the other with a PLE pulse. A multiplexer is provided for selecting the outputs from the two delay lines. Normally, the output of the ALE delay line is selected, while the PLE delay line is selected when a pseudo leading edge flag (PLEF) signal is applied to the multiplexer.

5. PSEUDO LE PULSE GENERATOR

When a reply is received, a condition may occur whereby two overlapping pulses are detected as one long pulse and the leading edge of the second pulse is not detected. The primary function of the pseudo LE pulse generator is to detect this condition and insert a pseudo leading edge (PLE) pulse into the LE pulse stream that is delivered to the memory delay. If a prolonged pulse is detected indicating that more than two overlapping pulses were detected, extra leading edge (XLE) pulses are generated and inserted into the LE pulse stream. An additional function is to provide encode command pulses to an A/D converter which is used to measure the monopulse off-boresight pulses. A functional block diagram of the pseudo LE pulse generator is presented in Fig. 5-1.

5.1 Leading Edge Pulse Propagation

Each actual leading edge (ALE) pulse received from the video digitizer passes through a minimum pulse width filter. If an actual trailing edge (ATE) pulse appears at this filter before a prescribed time has elapsed after the appearance of an ALE pulse (two clock-pulse periods), this filter prevents the ALE pulse from appearing at the filter output. ALE pulses resulting from reply pulses that exceed the minimum width requirements are permitted to pass through the filter to the LE pulse propagation line, to the ALE pulse encode command delay, and to the PLE pulse detector.

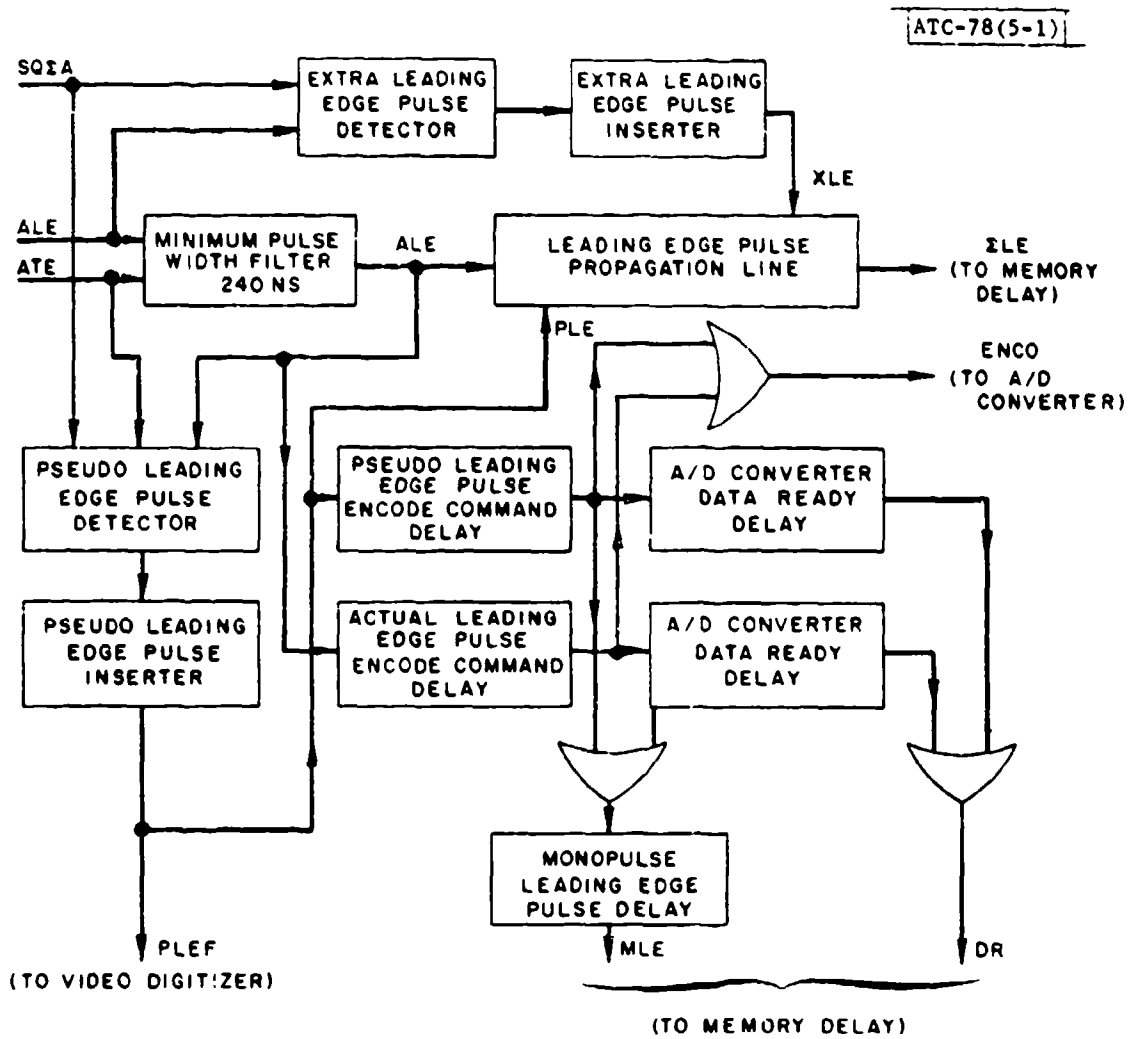


Fig. 5-1. Pseudo LE pulse generator, block diagram.

The ALE pulses entering the LE pulse propagation line are shifted down the line at the clock pulse repetition rate. Taps are provided in the line for inserting PLE and XLE pulses, as required. The output of the LE pulse propagation line (ΣLE) consists of a stream of LE pulses which may include inserted PLE and XLE pulses in addition to the ALE pulses. No distinction between these types of pulses is made at the output of this line.

5.2 Pseudo and Extra Leading Edge Pulses

One PLE pulse is generated for every SQΣA pulse whose duration exceeds that of a normal reply pulse. It is generated upon the termination of an SQΣA pulse and is inserted into the LE propagation line in such a manner that its relative position precedes the SQΣA pulse trailing edge by one normal reply pulse duration. Extra leading edge (XLE) pulses are generated when either the SQΣA pulse duration becomes much longer than the duration of a normal reply pulse or when an ALE pulse appears after the SQΣA pulse duration has exceeded that of a normal reply pulse. XLE pulses are inserted into the propagation line following the ALE pulse associated with the excessively long SQΣA pulse at intervals equal to one normal reply pulse duration. The insertion of XLE pulses continues until either an ALE or a PLE pulse appears on the propagation line.

5.2.1 Generation of Pseudo Leading Edge Pulses

The generation of pseudo leading edge (PLE) pulses is performed by the PLE pulse detector and the PLE pulse inserter. The PLE pulse detector essentially is a counter which is continuously being reset during the absence of an SQΣA pulse. When an SQΣA pulse appears at the detector, the counter begins to

count. However, for SQΣA pulses that equal or exceed the minimum pulse width requirements, the ALE pulse which emerges from the minimum pulse width filter resets the counter. The counter then starts again and continues counting for the duration of the SQΣA pulse. The counter is set so that it overflows when the SQΣA pulse duration exceeds 5 clock pulses - the duration of a standard reply pulse is 3 to 5 clock pulses. When an overflow occurs, the PLE pulse detector is conditioned to generate a PLE pulse upon the appearance of an ATE pulse.

The combination of a counter overflow condition and the appearance of an ATE pulse at the input to the PLE detector causes a PLE pulse to be forwarded to the PLE pulse inserter. The PLE pulse then is inserted into the LE propagation line such that its relative position precedes the trailing edge of the SQΣA pulse by 4 clock pulses which is the nominal reply pulse duration. At the same time, the output of the PLE pulse inserter is forwarded to the PLE pulse encode delay, and to the video digitizer as a PLE Flag (PLEF).

5.2.2 Generation of Extra Leading Edge Pulses

The generation of extra leading edge (XLE) pulses is performed by the XLE pulse detector and the XLE pulse inserter. The XLE pulse detector essentially consists of two counters that function in a manner similar to the counter in the PLE detector. One counter overflows when the SQΣA pulse duration equals nine clock pulses and activates the XLE pulse inserter. The other counter overflows when the SQΣA pulse duration exceeds five clock pulses, but it does not activate the XLE pulse inserter until an ALE pulse appears at the detector input. When activated, the XLE pulse inserter adds an XLE pulse into the

LE pulse propagation line at four clock-pulse intervals following the leading edge of the SQΣA pulse. This insertion process stops when the XLE inserter detects the appearance of an ALE or a PLE pulse in the propagation line.

5.3 A/D Converter Encode Command and Data Ready Signals

Encode commands for the monopulse off-boresight A/D converter are derived from the ALE pulses appearing at the output of the minimum pulse width filter, and the PLE pulses appearing at the output of the PLE pulse inserter. XLE pulses, however, are not used for this purpose. The ALE and PLE pulses are delayed by an amount that is appropriate for encoding the monopulse off-boresight reply pulse when it appears at the A/D converter. These encode command (ENCO) pulses are forwarded to the A/D converter and to the A/D converter data ready delay. The delay is equal to the interval required by the A/D converter to perform its function. The appearance of the Data Ready (DR) pulses at the output of this delay signify the completion of the A/D conversion, and are used to signal the memory delay that the A/D converter data are valid and should be read.

5.4 Monopulse Leading Edge Pulses

The monopulse leading edge (MLE) pulses are ALE and PLE pulses that have been appropriately delayed. The delay is such that the MLE pulses will arrive at the memory delay coincidently with its corresponding ΣLE pulse. The MLE pulses therefore flag these ΣLE pulse as having an associated monopulse value.

6. MEMORY DELAY

The primary function of this subsystem is to provide a 20.3 microsecond delay to the following signals:

a. ΣLE.

b. RSLSF.

c. The 8-bit value of the monopulse off-boresight pulse (ϕ_{AD}) obtained from the A/D converter.

Both the delayed and undelayed forms of these signals are forwarded to the reply controller. A secondary function is to buffer the 8-parallel-bit monopulse signal (ϕ_{AD}) so that it will be aligned with the monopulse leading edge (MLE) signal obtained from the PLE pulse generator. A functional block diagram of this circuit function is presented in Fig. 6-1.

The monopulse off-boresight signal (ϕ_{AD}) is buffered and aligned with the MLE pulse before entering the memory delay. The FIFO (first in, first out) buffer is a short 8-parallel-bit pulse propagation line operating at the clock pulse repetition rate and controlled by the buffer controller. Entry into the buffer occurs when a data ready (DR) pulse is present; otherwise, signal ϕ_{AD} is lost. Propagation out of the buffer is permitted only when the MLE pulse is present. Thus, if signal ϕ_{AD} arrives at the buffer output before its corresponding MLE appears, signal ϕ_{AD} is held at the buffer output until the MLE pulse arrives.

Propagation within the FIFO buffer is controlled by the buffer controller. The controller is a register which remembers the content of each propagation

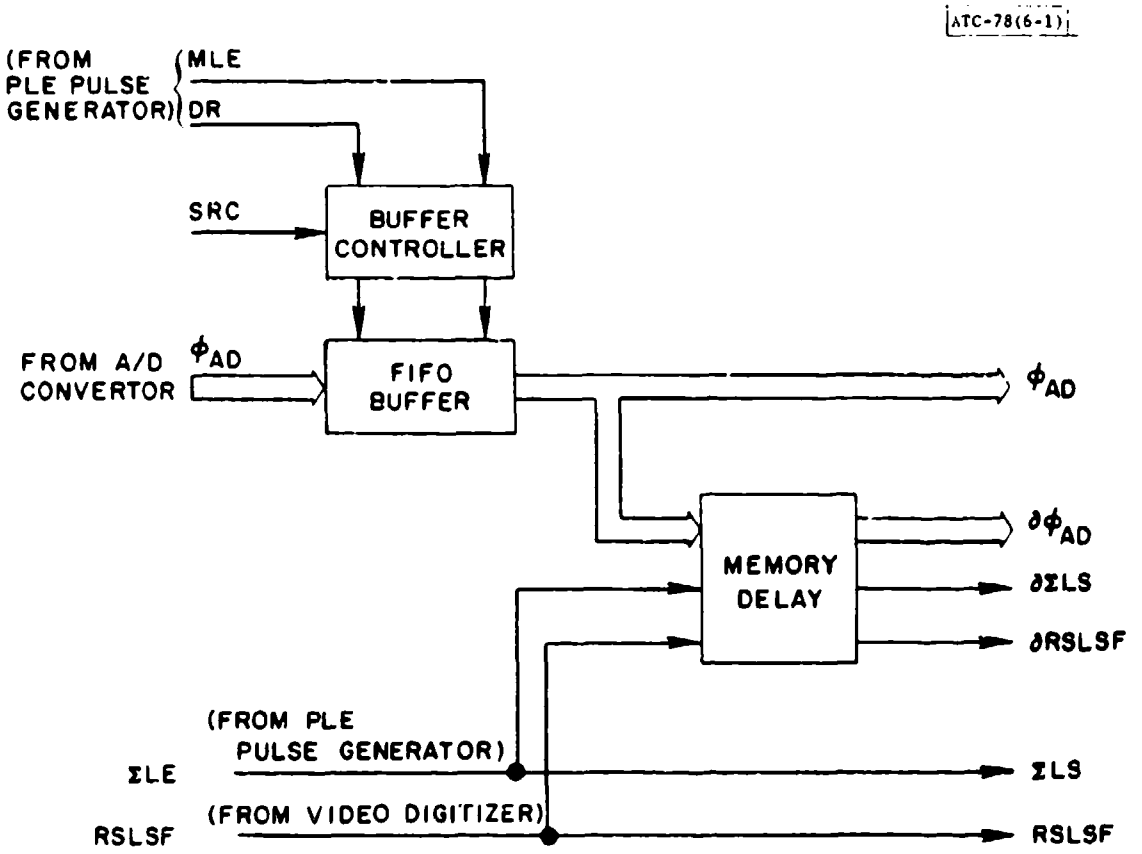


Fig. 6-1. Memory delay, block diagram.

element within the buffer and halts the propagation if the element preceding it is occupied. Such a condition would occur if there was an excessive holdup at the buffer output. The buffer controller is cleared by the SRC signal each time the range window opens.

The 20.3 microsecond delay for signal ϕ_{AD} and the RSLSF and ΣLE pulses is obtained via a set of dual random access memories. These memories operate in a ping-pong fashion whereby one memory stores the data while the data previously stored in the other memory are being read-out.

7. REPLY CONTROLLER

The primary functions of the reply controller are to detect the presence of an F_1, F_2 bracket pulse pair, select either the F_1 or F_2 pulse as the monopulse reference, and deliver the monopulse reply pulses to the decoders. A block diagram of this circuit function is presented in Fig. 7-1.

7.1 Bracket Pulse-Pair Detection

When an undelayed and a delayed ΣLE pulse appear simultaneously at the bracket detector, the separation interval between these two pulses meets the requirement for the presence of an F_1, F_2 bracket pulse pair. Unless the detection is inhibited, a bracket pulse pair declaration will be made in the form of a detection pulse appearing at the output of the bracket detector. The undelayed and delayed RSLSF lines indicate whether the corresponding ΣLE pulse was received in the antenna mainbeam or in a sidelobe. Absence of a pulse on the RSLSF line signifies that the corresponding ΣLE pulse was received from within an antenna sidelobe. The bracket detection pulse from the bracket detector normally passes through a pulse propagation delay line to the detector selector where a decoder is selected to receive the reply.

There are certain conditions under which bracket detection does not occur. These conditions are:

a. A previous bracket detection has occurred within two clock periods.

b. The bracket has been identified by one of the decoders as a C_2-SPI bracket.

c. A DABS preamble is detected in the received reply.

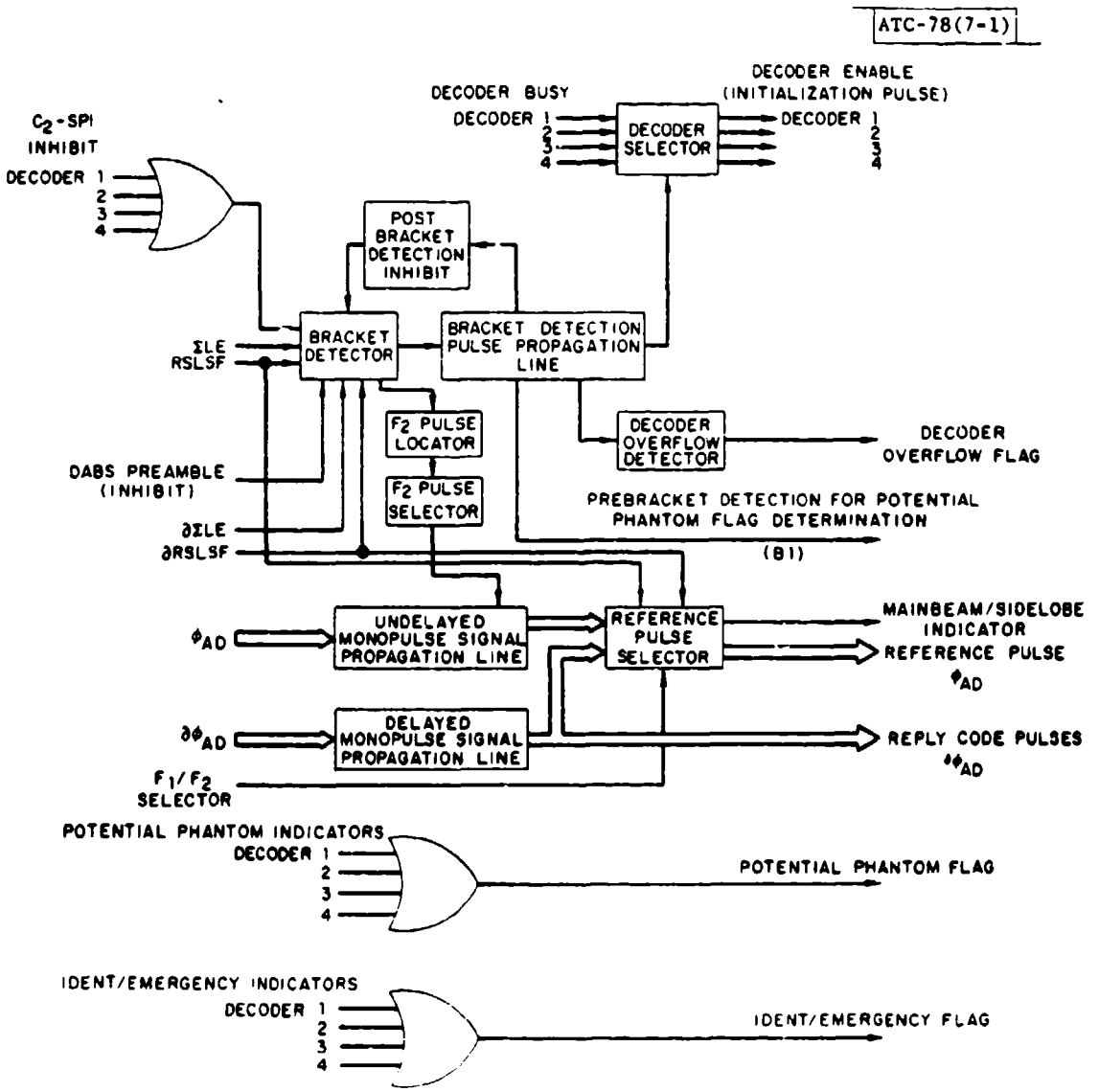


Fig. 7-1. Reply controller, block diagram.

7.2 Decoder Selection

After a bracket detection pulse is received by the decoder selector, it enables an inactive decoder to receive the reply data associated with this bracket detection. The reply data transferred to the decoder consist mainly of the 8 bit A/D converter reading (ϕ_{AD}) of each monopulse off-boresight-angle reply pulse that exists between the detected bracket pulses. After F_1 or F_2 is selected as the monopulse reference pulse, the delayed monopulse reply pulses are forwarded to all four reply decoders via a code pulse bus. These reply pulses then are accepted by the decoder that was enabled by the decoder selector. The decoder continues to accept pulses for the duration of the reply, and stops accepting pulses after the SPI pulse position has passed.

7.3 Reply Pulse Processing

Early in the bracket detection pulse propagation line, a tap is provided for splitting off a prebracket detection line to all four decoder boards. This prebracket detection line is used by the decoders to determine if the detection is a potential phantom. If the determination is that this detection is possibly a phantom, a potential phantom indication is sent to this circuit and arrives by the time that the bracket detection pulse has propagated to the decoder selector. This potential phantom flag then appears on the data bus going to the decoder along with the reply code-pulse data.

Another tap near the end of the bracket detection pulse propagation line goes to the decoder overflow detector. When a bracket detection pulse appears

at the detector and all decoders are busy, the reply data associated with this bracket detection are not permitted to enter any of the busy decoders and are lost. A decoder overflow signal is forwarded to the reply assembler to indicate the loss of these data.

When a reply is assigned to a reply decoder, a military ident/emergency bit may be sent to the reply decoder along with the initialization pulse to indicate that this particular reply may be a reply in a military ident (SPI) or a military emergency sequence. The meaning of the military ident/emergency bit (as generated by the reply controller with the help of timing information from the individual reply decoders) is that a reply is currently being processed by a decoder which was detected by the reply controller 24.65 $\pm$ 0.10 microseconds prior to the bracket which the controller is presently assigning.

7.4 Monopulse Reference Pulse Selection

Either the F_1 or the F_2 pulse is selected as a comparison reference against which each monopulse reply pulse will be matched. Before F_2 can be selected as a reference, its location with respect to F_1 must be known precisely. The desired degree of precision is obtained by monitoring the pulse propagation elements in the undelayed monopulse signal propagation line since the nominal precision used for bracket detection is inadequate. This monitoring is performed by the F_2 pulse locator. When a bracket detection occurs, the F_2 pulse locator is provided with an identification of the pulse propagation element containing the F_2 pulse. This identification is converted

to a precise measurement of the F_2 pulse location with respect to F_1, and this measurement together with its mainbeam/sidelobe indication is forwarded to the F_2 pulse selector. The F_2 pulse selector then adjusts the propagation elements in the undelayed monopulse signal propagation line in such a manner that the F_2 pulse appears at the reference pulse selector simultaneously with the F_1 pulse from the delayed monopulse signal propagation line.

The decision for using F_1 or F_2 as the reference pulse is made by the decoders. It is forwarded to the reference pulse selector in time to permit the selection.

8. REPLY DECODERS

Four identical reply decoders are used to permit the handling of up to four overlapping replies. After a decoder has been assigned to process a detected reply, every pulse detected during the reply interval is processed even though some of the pulses may be part of a reply being processed in one or more of the other decoders. A set of counters is used to determine precisely when each reply pulse should occur following the F_1 pulse. Only those decoded pulses that appear at the reply pulse processor output at the times specified by the counters are retained by the decoder. A block diagram of a decoder is presented in Fig. 8-1.

8.1 Reply Pulse Selection and Generation of Flags

The precise location of each pulse within a reply interval is measured by a set of counters located in the reply pulse selector. A 12-stage ring counter operating at the clock pulse rate is used to divide each inter-pulse period into 12 divisions. This division of the reply pulse period provides a means of determining whether or not the pulse being decoded coincides with a pulse being decoded in another decoder.

Because the time for each pass around the ring counter (1.4 μsec) is equal to a reply pulse period, the ring counter also provides a means of locating the position of every pulse within the reply. Consequently, three state counters are used in counting each ring-counter pass to obtain the position of the C_2, F_2, and SPI pulses with respect to the F_1 pulse. At the end of a reply interval (24.65 μs after the F_1 pulse - the SPI pulse is included in a decoder reply interval), the ring counter is stopped, and the reply assembler is notified that a four-word decoded reply message is ready for transfer.

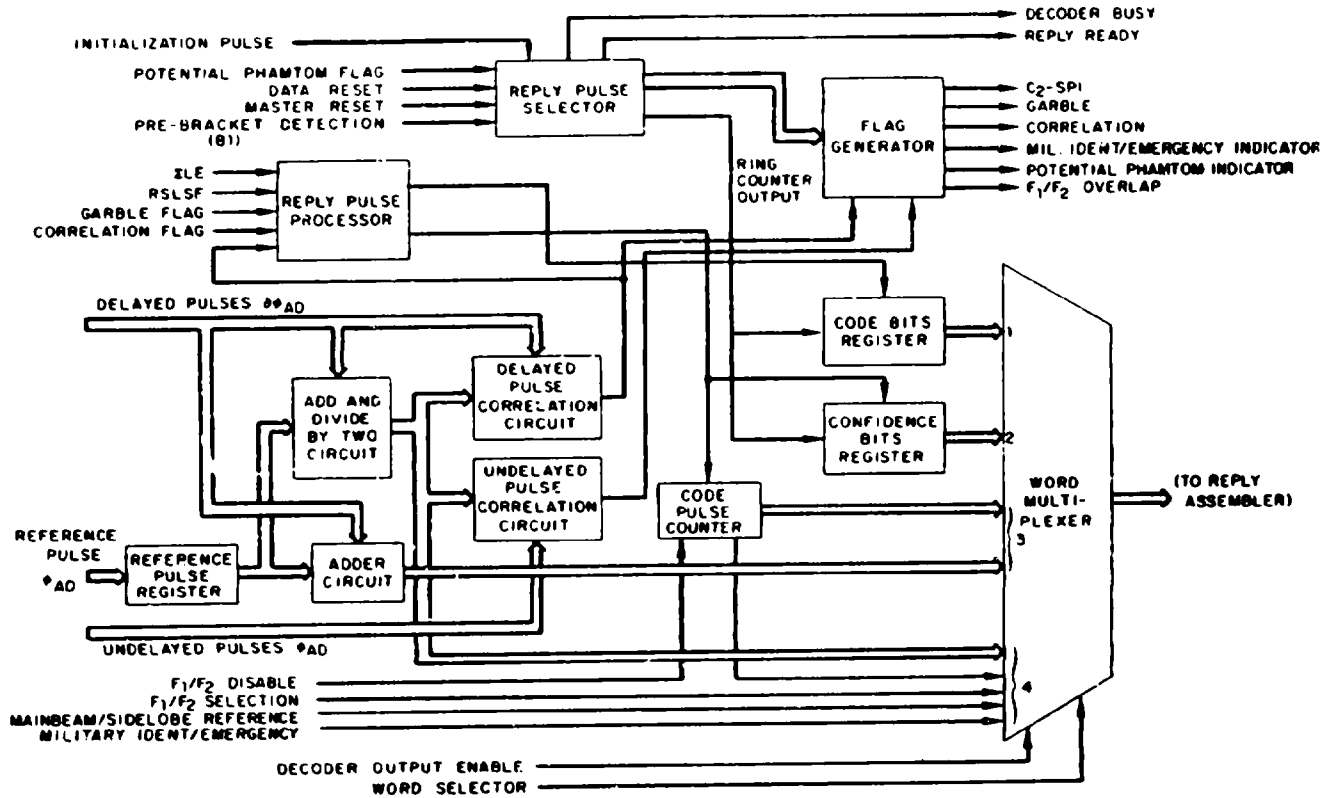


Fig. 8-1. Reply decoder, block diagram.

Inputs to the reply pulse selector are as follows:

a. Initialization signal from the reply controller.

b. Prebracket detection pulse from the reply controller.

c. Potential phantom flag from the other decoders.

d. Data reset signal from the reply assembler.

e. Master reset signal from the video digitizer upon detecting the start of a new sweep.

The initialization signal is received from the reply controller at the same time that the first reply pulse (F_1) is received. This signal starts the ring counter and associated state counters, and sets a flip-flop which sends a decoder busy signal back to the reply controller.

The prebracket detection signal and the potential phantom flag function collectively to suspend the operation of a decoder when the reply being decoded is determined to have been the result of a phantom detection. This determination is made when the reply being decoded is a potential phantom (the decoder's potential phantom flip-flop is set by the potential phantom flag) and the prebracket detection signal of a reply currently being detected is received. If the prebracket detection signal coincides with a particular five clock-pulse span - as measured by the ring counter - of a pulse being decoded, the decoder operation stops, the potential phantom flag and the decoder busy flip-flops are reset, and the reply controller is notified that this decoder is available for another reply. The data accumulated by the decoder before its operation was suspended are retained until they are overwritten by new data.

The data reset signal is set by the reply assembler after it receives all of the words from the decoder. This signal resets the decoder busy and potential phantom flag flip-flops. Resetting the decoder busy flip-flop also resets the state counters and every element in the ring counter. This resetting operation is also performed at the beginning of each reply listening interval by the master reset signal.

At specific intervals designated by the ring counter during the decoding of a reply, the decoder transmits flags to the other decoders and/or the reply controller. These other decoders utilize the flags when they are in the act of processing a reply. Six types of flags are generated by a decoder:

a. A potential phantom flag is issued to the reply controller when the decoder begins to process the F_1 reply pulse, and it is removed after the F_2 pulse has been processed. This flag has a duration of 20.75 μsec.

b. An F_1/F_2 overlap flag is issued to the reply controller at the beginning of every reply pulse duration. Its presence at the reply controller when a bracket pair is being declared specifies that the F_2 pulse be selected as the reference pulse for decoding purposes. This flag has a duration of five clock pulse intervals.

c. A C_2-SPI phantom flag is issued to the reply controller when the decoder is processing the C_2 reply code pulse and an SPI correlation is received from the undelayed pulse correlation circuit. This flag has a duration of three clock pulse intervals.

d. A garble flag is issued to the other decoders at the beginning of each reply pulse duration and at the beginning of the SPI pulse duration. This flag has a duration of three clock pulse intervals.

e. A correlation flag is issued to the other decoders at the beginning of each reply code pulse duration and at the beginning of the SPI pulse duration, provided that these pulses correlate with the reference pulse. An additional condition for the issuance of this flag is that both the reference pulse and the code or SPI pulses are not zero. This flag has a duration of three clock pulse intervals.

f. The military ident/emergency flag is issued to the reply controller at the beginning of the SPI reply pulse interval. This flag has a duration of three clock pulse intervals.

8.2 Reply Pulse Processing and Decoding

The reply pulse processing and decoding circuit consists of a reply pulse processor, a code bits register, a confidence bits register, and a code pulse counter. Inputs to the reply pulse processor are as follows:

a. Delayed leading edge pulses from the reply controller.

b. Delayed sidelobe suppression flag pulses from the reply controller.

c. Garble flags from each of the other active decoders.

d. Correlation flags from each of the other active decoders.

e. Correlation flag from this decoder.

The reply pulse processor receives every pulse that is present during a reply interval, even though some of these pulses may be part of a reply that is being decoded by another decoder. Each pulse is examined with respect to its associated sidelobe suppression, garble, and correlation flags that are present. Based upon this examination, the processor decodes the pulses as a one with either a high or low confidence factor. The decoding of a zero involves an examination of four pulse propagation elements (the nominal position, ± 1 position, and the position at nominal -2). Absence of a pulse is decoded as zero with a high confidence factor provided that no pulse is present in any one of these elements.

Each decoded pulse and its corresponding confidence factor pulse are delivered in a serial manner to the code bit register and the confidence bit register, respectively. However, an output from the ring counter in the reply pulse selector permits only those pulses occurring at 1.45 μsec intervals following the F_1 pulse to enter the registers. The output of each register is delivered in a parallel manner to the word multiplexer.

The code pulse counter counts the number of confidence bits associated with each reply pulse that is decoded as a one. This counter provides to the word multiplexer a four-bit parallel output of the total number of such decoded pulses. Derived from this counter is an indication that the number of pulses decoded as a one was a quantity of two or more, or did not exceed a quantity of two. This count is used later by the software algorithm to decide whether or not to use the monopulse estimate of this reply.

This counter is inhibited when the monopulse reference pulse appears at the code bit register.

8.3 Pulse Correlation and Off-Boresight Estimate Processing

The pulse correlation and off-boresight estimate processing circuit consists of an add-and-divide-by-two circuit, a reference pulse register, a delayed pulse correlation circuit, and an undelayed pulse correlation circuit. The add-and-divide-by-two circuit sums the A/D converter values of the delayed monopulse off-boresight pulse and the reference pulse, then divides the sum by two to obtain an average off-boresight value. The reference pulse, either F_1 or F_2, is selected at the reply controller and is received at the decoder reference pulse register. When the next off-boresight value appears, it is added to the previously computed average value and divided by two to obtain an updated average value. This add-and-divide-by-two process continues for the duration of the reply interval. The output of this circuit is delivered to the word multiplexer, and to the delayed and undelayed pulse correlation circuits.

The delayed pulse correlation circuit measures the difference between the A/D converter values of each delayed monopulse off-boresight pulse and the decoder-averaged reference pulse. A correlation exists between the two signals if the magnitude of the difference is less than or equal to an adjustable threshold level. Then a correlation pulse is generated and delivered to the reply pulse processor and to the flag generator.

The undelayed pulse correlation circuit measures the difference between the A/D converted value of each undelayed monopulse off-boresight pulse and the decoder-averaged reference pulse. A correlation between these two signals is obtained as in the delayed pulse correlation circuit, and a correlation pulse is delivered to the flag generator for use in generating the C_2-SPI flag.

The adder circuit is initialized to the value of the reference pulse register. Then, each subsequent off-boresight value is summed with the contents of this circuit for the duration of the reply interval. The output of this circuit is delivered to the word multiplexer. Numerically, the adder circuit produces a value equal to the sum of all monopulse values which contributed to the final monopulse estimate.

8.4 Output Word Multiplexer

The output word multiplexer provides a means of sequentially selecting the data processed or accumulated by the decoder for transmission to the computer as directed by the reply assembler. Enabling and the sequential word selection of the multiplexer are performed at the reply assembler. Word data appearing at the multiplexer are as follows:

Word 1: Code Bits. (16 bits)

Word 2: Code Confidence Bits. (16 bits)

Word 3:

a. Number of pulses which contributed to the final off-boresight value either is equal to or greater than two, or is less than two. (1 bit)

b. The reference pulse was F_1 or F_2. (1 bit)

c. The reference pulse was detected in the mainbeam or sidelobe. (1 bit)

d. The reply was normal or a military ident/emergency. (1 bit)

e. The final off-boresight estimate. (8 bits)

Word 4:

a. Number of pulses which contributed to the final off-boresight estimate. (4 bits)

b. Arithmetic sum of the values which contributed to the final off-boresight value. This was included to allow an evaluation of the performance of a uniform weighting function versus the weighting function specified in ER-26. (12 bits)

These words are shown as part of the reply message in Fig. 9-2.

9. REPLY ASSEMBLER

Two types of four, 32-bit word messages are assembled by this circuit for transfer to the computer interface:

a. Sweep header messages.

b. Reply messages.

A sweep header message is assembled at the beginning of every reply listening interval following the transmission of an ATCRBS interrogation by the ground sensor. The sweep header message is enabled by the sensor range gate signal and is always the first message transferred to the computer during the reply listening interval. After transfer of the sweep header to the computer is completed, the assembler either waits for notification from one of the decoders that a reply is ready, or it begins to transfer the message of a reply that was accumulated by the assembler while the sweep header message was being transferred. The reply processor has the capacity of accumulating four replies.

A detailed block diagram of the reply assembler is presented in Fig. 9-1. The format content of the message delivered to the computer interface is shown in Fig. 9-2.

9.1 Sweep Header Message

The primary elements involved in the assembly and transfer of a sweep header message are:

a. Sweep header flip-flop.

b. Word select counter.

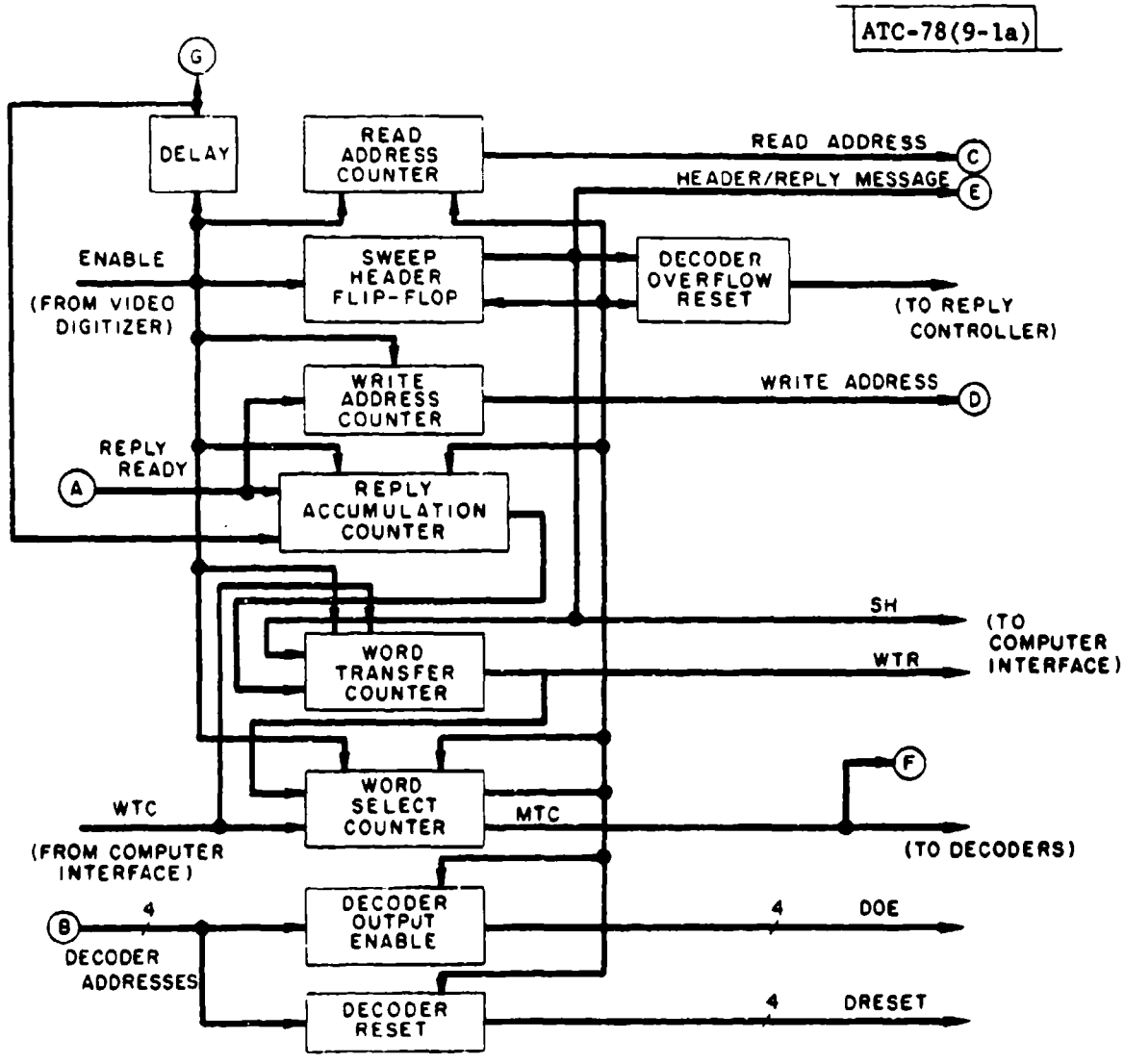


Fig. 9-1. Reply assembler, block diagram.

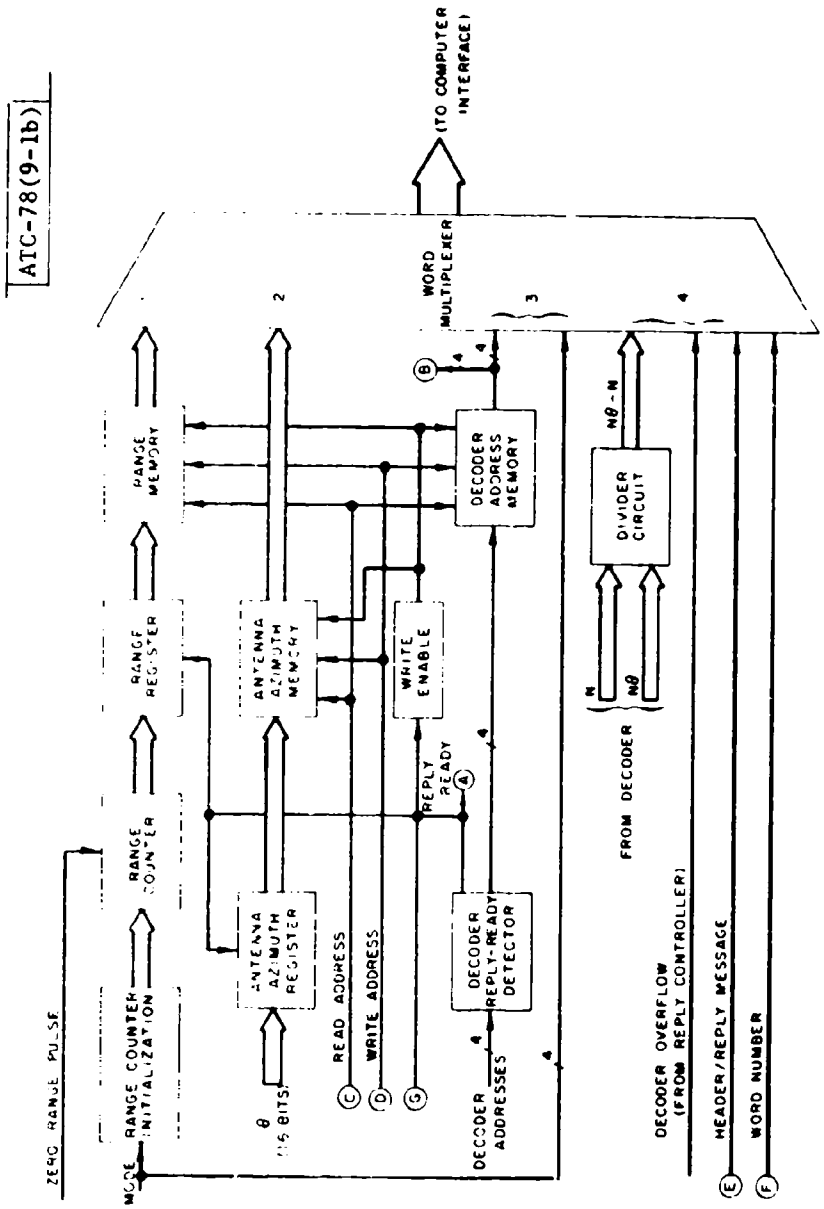


Fig. 9-1. (Continued)

ATC-78(9-2)

RANGE				CODE	
ANTENNA AZIMUTH				CODE CONFIDENCE LEVEL	
MODE	SPARE	SPARE	ADDRESS	SPARE	THETA
0 0 1 1	0 0 [redacted]	Nθ ÷ N		R	Nθ

Range: 16-bit reply range estimate with LSB = 60.4 nsec.

Code: Reply decoder output.

Antenna Azimuth: Antenna pointing direction at bracket detection.

Code Confidence: Decoder confidence level associated with each code bit. { 1 = high / 0 = low

Mode: Interrogation mode type.

Address: An indication of which one of four decoding registers processed this reply.

Theta: The final off-boresight monopulse estimate.

$\bar{N}$: Number of pulses which contributed to the final off-boresight monopulse estimate.

$N\theta$: The arithmetic sum of the monopulse values which contributed to the final value.

$N\theta \div N$: Number divided by N (division done by the processor).

$N\theta \div N$ is included to allow an evaluation of the performance of a uniform weighting function versus the weighting function specified in ER-26 to produce Theta.

1. Bit = 1 if $N > 2$
   = 0 otherwise
2. Bit = 1 if F1 was the monopulse initialization pulse
   = 0 if F2 was the monopulse initialization pulse
3. Bit = 0 if the monopulse initialization pulse was mainbeam
   = 1 if the monopulse initialization pulse was sidelobe
4. Bit = 0 if the Military SPI/Emergency bit was set
   = 1 otherwise
5. Bit = 1 if decoder overflow occurred during the previous sweep
   = 0 otherwise
6. Bit = 1 if this 4 word data block is a sweep header
   = 0 if this 4 word data block is a reply report

[ ] Data used in the sweep header message

[ ] Data from a decoder

Fig. 9-2. Message format and content.

c. Word transfer counter.

d. Word multiplexer.

e. Decoder overflow reset.

Also used are the elements involved in obtaining the antenna azimuth and range count at the moment that the range gate is initiated.

As shown in Fig. 9-2, the data generated for use in the sweep header message are:

a. Range (state of the range counter when the range gate was initiated.)

b. Antenna azimuth.

c. Interrogation mode.

d. Previous-sweep decoder-overflow indication.

e. Sweep header message indication.

Initiation of a sweep header message occurs when the reply assembler receives, from the video digitizer, an enable signal derived from the beginning of the range gate. The enable signal sets the sweep header flip-flop and resets the word select counter. It also resets the read address, the write address, the reply accumulation, and the word transfer counters in preparation for their use in assembling the sweep header message.

The delayed portion of the enable signal sets the antenna azimuth and the range registers, then activates the write enable circuit causing the contents of the antenna azimuth register, the range register, and the decoder

reply-ready detector to be deposited into their corresponding memories. (No decoder addresses are detected for the sweep header message.) Because the read address and the write address counters were both set to zero, the data written into the memories are read out to the word multiplexer at the instant that they are written. In addition, the delayed enable signal acts as a reply enable signal (see Section 9.2) and causes a one to be shifted into the reply accumulation counter.

Selection of the words appearing at the word multiplexer for transfer to the computer interface is performed by the word select counter. After being reset by the enable signal, the word select counter selects the first word at the word multiplexer for transfer to the computer interface. Then, each time a word transfer complete (WTC) signal is received from the computer interface, the counter increments and selects a new word at the multiplexer for transfer. Upon receipt of the WTC signal after the transfer of the fourth word has occurred, the counter increments once more and issues a message transfer complete (MTC) signal. The MTC signal resets the word select counter in anticipation of a subsequent reply message, and activates a decoder overflow reset signal (sent to the reply controller) just prior to resetting the sweep header flip-flop.

The word transfer counter operates in conjunction with the word select counter to provide a short delay between the time that a word has been selected for transfer and the time that the word transfer is requested. After the word transfer counter is reset to a predetermined value by the enable signal, the set condition of the sweep header flip-flop and the presence of a one in the reply accumulation counter enable the word transfer counter.

Upon completion of the count, the output is used as a word transfer request (WTR) signal for the word specified by the word selector counter. This WTR signal is forwarded to the computer interface circuit, provided that a WTC signal is not present at the input to the word transfer counter. The WTR signal also removes the enabling signal to the word transfer counter, thereby permitting the WTC signal, when it appears, to reset the counter. Resetting the word transfer counter restores the enabling signal to this counter and permits the counter to being its counting cycle.

After the fourth word has been transferred, the word transfer counter begins its counting cycle as usual upon receiving a WTC signal. However, the MTC signal from the word select counter resets the sweep header flip-flop and shifts out the one in the reply accumulation counter at the instant that the word transfer counter is one count short of completing its counting cycle. Because the resetting action of the sweep header flip-flop and the absence of a one in the reply accumulation counter remove the enabling signal from the word transfer counter, the counter stops and waits for the initiation of a reply message to complete its counting cycle.

Antenna azimuth is derived from a shaft encoder located on the interrogating antenna pedestal via a serial to parallel azimuth accumulator. The accumulating azimuth value is continuously applied to the antenna azimuth register so that the register will always reflect the latest encoder reading. To provide correct synchronization, the azimuth register is not permitted to change values:

a. During the time that the shaft encoder value is changing.

b. During the time that data are being transferred from the antenna azimuth register to the antenna azimuth memory.

Range is derived from a free running range counter located in the reply assembler. At the beginning of a sweep, a zero range pulse resets the range counter to an initial value. At the instant that the delayed enable signal is applied to the range register, the range counter reading is transferred to the range register for subsequent writing into the range memory.

9.2 Reply Messages

Reply messages are issued after the transfer of the sweep header message is completed and upon receipt of a reply ready signal from a decoder that has finished decoding a reply. Selection of a word for transfer to the computer interface occurs in a manner identical to that of the sweep header message words, except that the words are transferred from both this circuit and the decoder which has the reply. A decoder output enable (DOE) signal issued to a decoder enables the decoder word multiplexer to transfer its word simultaneously with the word from this circuit. The reply assembler contributes the following data to the total message block (see Section 8 for a description of the data which is simultaneously coming from the decoder):

a. Range of the reply.

b. Antenna azimuth at the time of reply detection.

c. Decoder from which data were obtained.

d. Reply message indication.

e. Quotient of the arithmetic sum of the monopulse values which contributed to the final off-boresight estimate divided by the number of pulses that contributed to the estimate.

It should be noted that the interrogation mode and decoder overflow bits are not used in a reply message.

When a reply-ready signal appears on one of the four decoder address lines, it is detected at the address line goes high at the decoder address memory. Then, the output of the decoder reply-ready detector is applied to the antenna azimuth register, the range register, the write enable circuit, the write address counter, and the reply accumulation counter. The write address counter increments and a one is shifted into the reply accumulation counter. A one in the reply accumulation counter enables the word transfer counter. Because the word transfer counter stopped at one count prior to completing its counting cycle after the previous message transfer was completed, the enable signal from the reply accumulation counter causes the word transfer counter to complete its count. Upon completing the count, a word transfer request (WTR) signal is forwarded to the computer interface, and the word select counter is enabled so that it will accept the word transfer complete (WTC) signal when it is received from the computer interface. The word select counter implements the transfer of the four words in the reply messages in the same manner that the transfer of the sweep header message was implemented.

The reply accumulation, the write address, and the read address counters permit the storage of up to three additional reply-ready data in the decoder address, the antenna azimuth, and the range memories while a message is being transferred to the computer interface. The reply accumulation counter registers the number of decoded replies that are ready for transfer. This counter essentially

is a four-bit shift register. Each time a reply is received, a one is shifted into this counter. Each time an MTC signal is issued by the word select counter, a one is shifted out of this counter. A maximum of four reply-ready counts can be stored in the counter. The presence of a reply-ready count causes a signal (from the word transfer counter) to be present at the word select counter which enables the word select counter to be incremented whenever a WTC signal appears.

The write address counter is a four-bit circular counter which specifies the location within the range, the antenna azimuth, and the decoder address memories where data are to be stored. A new memory address is specified each time the write address counter is incremented by the reply-ready signal. Just prior to incrementing the write address counter, the reply-ready signal is used to produce a write enable signal which implements the writing of data into the memories at the address specified by the counter.

The read address counter is a four-bit circular counter which selects the address of the range, the antenna azimuth, and the decoder address memories from which data are read out to the word multiplexer. This counter is incremented each time an MTC signal is issued by the word select counter and the data appearing at the new address are read out immediately.

At the beginning of each sweep, the read and write address counters are reset to zero. After the sweep header message transfer to the computer interface has been completed, the state of both counters is identical since each counter was incremented once during the transfer of the sweep header message. When the first reply is received at this circuit board, the antenna azimuth, range,

and decoder address data are written into the memories, then the write address counter is incremented. Because the states of the read and write address counters were identical before the write counter was incremented, the data are read out of the memories at the instant that they are written. If the replies accumulate faster than the transfer of messages, the read address counter will lag the write address counter until the accumulation of replies is depleted.

The decoder address, the antenna azimuth, and the range memories each permit the read-out of data at one address simultaneously with the write-in of data at another address. When a decoder has indicated to the reply assembler that it has a reply which is ready for transfer to the computer interface, the address of this decoder is stored in the decoder address memory. When an address is read out of this memory, it passes through a decoder output enable (DOE) circuit and forwards an enable signal to the addressed decoder where the decoder word multiplexer is enabled for the duration of the reply message transfer. When the message transfer has been completed, the MTC signal removes the enable signal from the decoder word multiplexer, and a decoder reset circuit sends a signal to the decoder for the purpose of releasing the decoder to process additional replies.

The antenna azimuth and range memories write the contents of their respective registers into the memory address directed by the write address counter. When this address is specified by the read address counter, the contents of the memories at this address are read out to the word multiplexer.

The divider circuit is used as a supplementary method of calculating the final off-boresight estimate. The 12-bit dividend from the decoder is

the arithmetic sum (Nθ) of the monopulse values which contributed to the final value. The four-bit divisor from the decoder is the number of pulses (N) that contributed to the final value. The eight-bit quotient (Nθ $\div$ N) is forwarded to the word multiplexer for transfer to the computer interface.

10. CLOCK CIRCUIT

The clock circuit provides the timing pulses necessary to operate all of the circuits contained in the ATCRBS Reply Processor. In addition, the clock circuit receives the garble and correlations flags issued by a decoder and distributes them to the other decoders. A block diagram showing the contents of this circuit is presented in Fig. 10-1.

A 16.552 MHz oscillator is used as the source for all of the timing pulses. The timing pulses at this frequency only are used to operate the range counter located in the reply assembler. Timing for all other functions occurs at one-half this frequency, i.e. 8.276 MHz.

Distribution of garble and correlation flags to the decoders is performed by the garble flag and correlation flag distributors, respectively. A flag received by its corresponding distributor from one of the decoders is channelled by the distributor to each of the three other decoders.

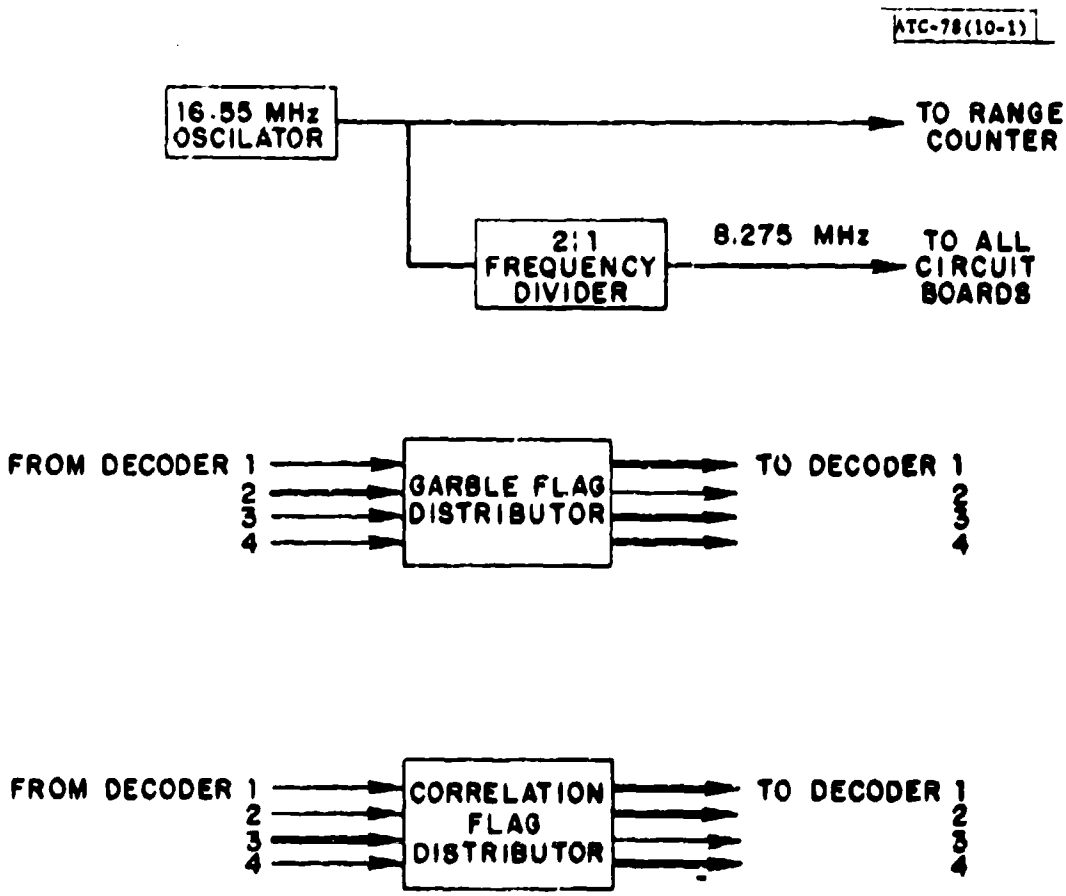


Fig. 10-1. Clock circuit, block diagram.

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2. J. L. Gertz, "The ATCRBS Mode of DABS," Project Report ATC-65, Lincoln Laboratory, M.I.T. (31 January 1977), FAA-RD-76-39, DDC AD-A038543/5.

3. Development of a Discrete Address Beacon System Quarterly Technical Summary, Lincoln Laboratory, M.I.T. (1 January 1976), pp. 5-12, FAA-RD-76-10, DDC AD-A023065/6.